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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,304	09/16/2003	Kallol Bera	8477/ETCH/DRIE	1356

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EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,304	BERA ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-17 and 40-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 40-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-17 and 40-45 have been considered but are moot in view of the new ground(s) of rejection.

2. The finality in the office action mailed 05/17/2005 is withdrawn. The new finality is made in this office action based on the amendment filed 03/15/2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-17 and 40-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. US 6,797,633 B2 in combination with Ma et al. US 2004/0161930 A1, Ideka US 6,426,299 B1, Chun et al. TW 544815 A and Samukawa et al. US 6,177,146 B1.

Re claim 1 and 40, the Jiang et al. reference discloses a method of fabricating an interconnect structure, which "may be the first or any subsequent metal interconnect level of the semiconductor device 120" (col. 3, lines 24-26), comprising:

(a) providing (first metal interconnect level of the semiconductor device 120 being formed) a substrate 100 having a film stack comprising sequentially formed on the

substrate a first barrier layer 101, a conductive layer 124 embedded in a first dielectric layer 102/104 (fig. 1F), (subsequent metal interconnect level of the semiconductor device 120 being formed) a second barrier layer 101, a second dielectric layer 102/104, and a cap layer 105 (fig. 1A);

(b) etching a via hole 106 in the cap layer and the second dielectric layer 102/104 (fig. 1C);

(c) filling a portion of a depth of the via hole with a masking material 107 (fig 1D);

(d) etching in-situ the cap layer 105, a trench 108 in the second dielectric layer 102/104, the masking material 107, and the second barrier layer 101(figs. 1E and 1F); and

(e) metallizing the via hole and the trench (fig. 1F).

The Jiang et al. reference discloses substantially all of the steps of the instant invention, teaches the use of O_2 plasma and other chemistries with or without inert gases to treat low-k films without damage to the OSG film but remove the resist (col. 3, lines 45-67) "[t]he exposure energy required to clear resist inside a via is the lowest for the wafer with in-situ O_2 plasma ash, indicating the most robustness for fighting poisoning" (col. 4, lines 15-26).

Re claim 2, the Jiang et al. reference teaches wherein the cap layer comprises SiO_xN_y, where x and y are integers (col. 3, line 40).

Re claims 3 and 41, the Jiang et al. reference teaches wherein the first dielectric layer and the second dielectric layer comprise at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass (col. 3, lines 28-36).

Re claim 4, the Jiang et al. reference teaches wherein the first barrier layer and the second barrier layer comprise at least one of SiO_2, SiC and Si_3N_4 (col. 1, line 52).

Re claim 5, the Jiang et al. reference teaches wherein the conductive layer comprises at least one of Cu, Al, Ta, W, Ti, TaN and TiN (col. 2, line 41).

Re claim 6, the Jiang et al. reference teaches wherein the masking material is selected from a group consisting of an organic material and photoresist (col. 4, lines 9-14).

Re claim 8, the Jiang et al. reference teaches wherein the step (c) further comprises: applying the masking material 107 to the substrate to fill the via hole 106; and etching back the masking material 107 until the masking material is removed from the via hole to a pre-determined depth that is smaller than a depth of the trench (col. 4, lines 9-15).

Re claims 9 and 42-43, the Jiang et al. reference teaches wherein the etching step further comprises: providing O_2 at a flow rate from about 100 to 1000 sccm; maintaining a chamber pressure at about 5 to 200 mT; and applying a cathode bias power between 100 and 400 W (col. 3, lines 1-4).

Re claim 10, the Jiang et al. reference teaches wherein the step (d) further comprises: forming on the cap layer a second patterned etch mask 132 to define the trench 108; and stripping the second patterned etch mask 132 contemporaneously with etching the masking material (col. 4, lines 27-30).

The four sub-steps in step (d) of Jiang et al. are summarized as "[t]rench pattern 132 and BARC 107 are then removed. The capping layer 105 and etch stop layer 101

are removed next during and etch stop etch" (col. 4, lines 28-30) without details of VHF frequency, bias power at a frequency, or source power and the ratio of CF_4:N_2 in each sub-step (*re claims 11-17 and 44-45).*

The Jiang et al. reference lacks providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts during at least a portion of etching period.

The Ma et al. reference discloses in-situ discharge to avoid arcing during plasma etch method wherein an inert gas and an etching gas are flowed into the chamber during the etching sequence (figs. 2-5) wherein the power is between 100 and 1000 Watts while chamber pressure is held between 20 and 150 mTorr [0028], a fluorocarbon gas $C_xF_yH_z$ where x and y are integers equal or greater than 1 and z is either 0 or an integer equal or greater than 1; the flow rate of fluorocarbon gas is between 0 and 50 sccm may be combined with N_2 and other fluorocarbon gas, the flow rate of the additional gas is also from 0 to 50 sccm, the same RF power, chamber pressure and time period apply in one step as in the other previous step [0029], the choice of gas for the discharge may be a matter of convenience [0033].

The Ideka reference discloses a method of etching the structure of fig.3 wherein a SiON 103, a SiO_2 104, an organic ARC 105 and a photoresist pattern 106 formed in that sequence on the base 101 with plug 102 embedded to reduce the F radicals (col. 1, lines 28-29 and col. 2, lines 35-37). The method in fig. 4 discloses plasma source power

of at least about 1000 Watts and a bias power of at least about 800 Watts during at least a portion of etching period.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the sub-steps of Jiang et al. with the power, pressure and flow rates as taught by Ma et al. and/or Ideka *to provide a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts during at least a portion of etching period according to the choice of gas as suggested by Ma et al.* and/or Ideka because the power, pressure and flow rates as suggested/taught by Ma et al. and/or Ideka would provide the sub-steps of Jiang et al. with in-situ discharge to avoid arcing during plasma etch processes and to reduce the F radicals which form a hardened surface layer.

The combination lacks an indication of the frequency of the VHF; however, Samukawa et al. teaches that the etching by exposing to plasma has been widely applied since it is highly practicable. High-density plasma etching generated in the course of electric discharge caused by applying an electric field of high frequency ranging in VHF to UHF bands, nearly from 100 to 1,000 MHz (col. 1, lines 20-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of the combination with an appropriate VHF frequency as taught by Samukawa et al. The use of frequency ranging in VHF to UHF bands in plasma etching is well known to those skill in the art as taught by Samukawa et al.

The combination lacks the ratio of CF_4:N_2 in a range from 1:1 to 1:5 in forming the via hole, *re claim 7.*

Re claim 7, the Jiang et al. reference discloses in the step (b): forming a first patterned etch mask 130 on the cap layer 105 to defined the via hole 106; etching the via hole; and stripping the first patterned etch mask (figs. 1C and 1D).

The Chun et al. reference teaches etching through a cap layer on the dielectric layer using N_2 and CF_4 in the ratio of 0-10:1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the via hole etching of the combination with the ratio of CF_4:N_2 as taught by Chun et al. because that ratio of Chun et al. would improve the etching of nitride to oxide layer as taught by Jiang et al.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Applicant's amendment filed on 03/15/2005 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP
08/01/2005

George Fourson
Primary Examiner